B5

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,014	03/06/2001	David Xiao Dong Yang	P-022	3849

32566 7590 09/10/2004

PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

EXAMINER	
YE, LIN	

ART UNIT	PAPER NUMBER
2615	3

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/801,014	Applicant(s) YANG ET AL.	
	Examiner Lin Ye	Art Unit 2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-30* is/are allowed.

6)☒ Claim(s) *1-6,9-17 and 21-23* is/are rejected.

7)☒ Claim(s) *7,8 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 objected to because of the following informalities:

   For claim 1, in page 21, line 7, the "**petitioned**" should be --**partitioned**--.

   Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   > (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 9-10, 12-14 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneyama J.P. Publication 04-313949 in view of Hynecek et al. U.S. Patent 6,229,133.

   Referring to claim 1, the Yoneyama reference discloses in Figures 1-6, an image sensor device comprising: a sensor array (image sensor 11, see page 7, [0012]) that outputs data signals representing one or more images of a scene (see page 5, [0008]); a memory space in communication with the sensor array (11), the memory space petitioned into a data memory (14, see page 7, [0011]) and a threshold memory (comparison circuit 17 has the standard value V1 for comparing the image data value of each pixel output from sensor array, see page 7, [0011] and page 9, [0015], lines 4-5), the data memory comprising memory cells for storing values representing the data signals; the threshold memory, in communication with

the sensor array, for storing threshold values (standard value V1) corresponding to each of the memory cells; and an updating mechanism (control circuit 19, see page 8, [0014]) for updating the data memory for each of the one or more images; the update mechanism causing a group of the memory cells to be updated even though only a fractional number of the memory cells (Mj) in the group need to be updated with new data signals (e.g.. it only stores the respective output value of the pixel elements do not exceed the standard value V1 and the count memory is not N to the corresponding areas in the data memory 14, see page 9, [0016]). However, the reference does not explicitly states the sensor array and memory space are fabricated in an integrated circuit.

The Hynecek reference discloses in Figures 1-4 and 8, the two-dimensional array (40, in Figure 2) is fabricated in an integrated circuit has a plurality of pixels (42-57 contain the device shown in Figure 1, see Col. 3, lines 1-14); the each of the pixel has a comparator circuit comprising a threshold memory (comparator 24 in Figure 1, 252 in Figure 8) for comparing if any pixel data associated with a pixel element exceed a predetermined threshold value (V_{REF}), the threshold memory for storing a threshold values corresponding to each of the memory cells (memory 26 in Figure 1, 254 in Figure 8) (Comparison result) for each of the pixel elements. The Hynecek reference is an evidence that one of ordinary skill in the art at the time to see more advantages for integrating sensor, control circuit and memory into a single integrated circuit, because it will significantly reduce the device size and making the device more portable; and the image sensor is a two-dimensional array so that the sensor array is more compact and easy to access. For that reason, it would have been obvious to

see the two-dimensional sensor array and memory space are fabricated in an integrated circuit disclosed by Yoneyama.

Referring to claim 2, the Yoneyama reference discloses wherein the updating mechanism (19) comprises: an identifying mechanism for identifying locations of the fractional number of the memory cells to be updated (e.g., 'j' denotes the picture element number of image sensor 11, 'Mj' denotes the location of memory cells, 'Nj' denotes the data of 'j' the pixel element stored in the count memory. When value 'Nj' contains N, it indicates the 'j' location of the memory cell need to be updated, see pages 9-10, [0015]-[0017]).

Referring to claim 3, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claim 1-2, and the Hynecek reference discloses wherein the identifying mechanism includes one of (i) a row counter (decoder 70) and (iii) a column counter (latch 74) (See Col. 3, lines 7-20).

Referring to claim 4, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claim 1-2, and the Yoneyama reference discloses wherein the group of memory cells (the corresponding areas in the data memory 14) is either a row of memory cells or a column of memory cells in the data memory (i.e. Mj is the data in the data memory 14 of jth picture element corresponding to the column or row).

Referring to claim 5, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claim 1-2, and the Yoneyama reference discloses wherein the identifying mechanism includes the threshold memory (comparison circuit 17) space that includes a number of cells, each corresponding to one of the memory cells in the data memory space (data memory 14); and wherein the fractional number of the

memory cells are updated with the new data signals when threshold values in some of the corresponding cells in the threshold memory space permit such updating (image output value not exceed the standard value V1) (See pages 9-10, [0015]-[0019]).

Referring to claim 9, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claim 1, and the both references disclose a two-dimensional array (the array has a plurality of columns and rows), so the sensor array is N by M pixels and provides pixel data in k bits, said data memory is N by M by k bits (the data memory 14 is for storing image data k bits for each of the pixel) and said threshold memory is at least N by M bits (e.g., threshold memory is simple and stores only a single bit of data, therefor the whole N by M pixels of sensor array has the N by M bits threshold memory).

Referring to claim 10, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claim 1, and the Yoneyama reference wherein the sensor array includes a plurality of pixel elements, each including a photo detector and an analog-to-digital conversation circuit (A/D 12), the photo detector generating an analog signal when the sensor array is exposed to the scene, the analog signal converted within the pixel element by the analog-to-digital conversation circuit to one of the data signals (See Page 7, [0012]).

Referring to claim 12, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 13, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claim 2.

Referring to claim 14, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claim 13, and the Yoneyama reference discloses identifying locations within a row of the data memory having a value that exceeds a predetermined threshold (V_1) that are to be updated (i.e. the first readout value $V_{A,1}$ shown in Fig. 6, exceeds the threshold value V_1, the count memory is updated to 1 instead of N).

Referring to claim 21, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claims 9 and 12.

Referring to claim 22, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claims 9 and 12.

Referring to claim 23, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claim 12, and the Yoneyama reference discloses providing the threshold memory for preventing read out of unnecessary values (i.e. as picture elements having saturated) to the data memory (see page 4, [0004]).

4. Claims 6 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneyama J.P. Publication 04-313949 in view of Hynecek et al. U.S. Patent 6,229,133 and Dill U.S. Patent 4,541,075.

Referring to claims 6 and 15-16, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claims 1-2 and 12, except that the reference do not explicitly show a read out mechanism for reading data out the group of memory cells (i.e., a row of the data memory) to a first buffer or other short term storage area within the image sensor device.

The Dill reference discloses in Figures 2-3, a method to access an integrated circuit semiconductor memory device. The integrated circuit device comprises a main memory (11); and a row buffer serial registers (25) including a first I/O port (23) for transferring (reading) the row from the main memory (e.g., this can be considered as a first buffer for reading data out a row of the data memory, see Col. 3-4, lines 65-67 and 13-17). The Dill reference is an evidence that one of ordinary skill in the art at the time to see more advantages for the image sensor device having a mechanism that utilizes a row buffer for storing the data read out of a row of the data memory so that significantly reduce a time sharing the memory between updating information to be reading out data and written into the memory (See Col. 2, lines 29-33). For that reason, it would have been obvious to see a read out mechanism for reading data out the group of memory cells (i.e., a row of the data memory) to a first buffer or other short term storage area within the image sensor device disclosed by Yoneyama.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneyama J.P. Publication 04-313949 in view of Hynecek et al. U.S. Patent 6,229,133 and Zhou et al. U.S. Patent 5,909,026.

Referring to claim 11, the Yoneyama and Hynecek references disclose all subject matter as discussed with respected to same comment as with claims 1 and 10, except that the references dos not explicitly disclose the integrated circuit is fabricated by a CMOS process instead of CCD.

The Zhou reference discloses in Figure 1, the integrated circuit (100) is fabricated by a CMOS process including a sensor array (112) and a frame memory array (130) (See Col. 3,

lines 24-30). The Zhou reference is an evidence that one of ordinary skill in the art at the time to see more advantages for the image sensor device can be fabricated by a CMOS process instead of CCD so that reduces the cost of manufacturing and power consumption (See Col. 1, lines 36-45). For that reason, it would have been obvious to see the Yoneyama's image sensor integrated circuit is fabricated by a CMOS process.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneyama J.P. Publication 04-313949 in view of Hynecek et al. U.S. Patent 6,229,133, Dill U.S. Patent 4,541,075 and Zhou et al. U.S. Patent 5,909,026.

Referring to claim 17, the Yoneyama, Hynecek and Dill references disclose all subject matter as discussed with respected to same comment as with claim 16, except that references do not explicitly show a short-term storage area within the image sensor for storing new data to be written from the sensor array to the data memory.

The Zhou reference discloses in Figure 1, the integrated circuit (100) is fabricated by a CMOS process including a sensor array (112), a frame memory array (130) and a column buffer (short term storage area) for storing new data to be written from the sensor array to the data memory (See Col. 3, lines 24-30). The Zhou reference is an evidence that one of ordinary skill in the art at the time to see more advantages for the image sensor device has a short term storage area within the image sensor for storing new data to be written from the sensor array to the data memory so that image data can be sequentially transfer from image sensor row by row without lost any previous row of data into the frame memory. For that reason, it would have been obvious to see the short-term storage area within the image sensor

for storing new data to be written from the sensor array to the data memory disclosed by Yoneyama.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

   A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

   Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1 and 12 (Application No. 09/801,014, hereinafter referred to as '014) provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 35, 42 and 46 of copending Application No. 09/567,786 (Hereinafter referred to as '786) in view of Yoneyama J.P. Publication 04-313949.

   This is a provisional obviousness-type double patenting rejection.

   Relative to claims 1 and 12 of '014 with claims 35, 42 and 46 of '786, the most limitations of claims are same as each other, such as sensory array for generating multiple representation of a scene at a plurality of exposure time, data memory, threshold memory, etc.; except the claims 35, 42 and 46 of '786 does not explicitly state a update mechanism

causing a group of the memory cells to be updated even though only a fractional number of the memory cells in the group need to be updated with new data signals.

Both claims are not distinct from each other, the Yoneyama reference discloses in Figures 1-6, an image sensor device comprising: a sensor array (image sensor 11, see page 7, [0012]) that outputs data signals representing one or more images of a scene (see page 5, [0008]); and an updating mechanism (control circuit 19, see page 8, [0014]) for updating the data memory for each of the one or more images; the update mechanism causing a group of the memory cells to be updated even though only a fractional number of the memory cells (Mj) in the group need to be updated with new data signals (e.g.. it only stores the respective output value of the pixel elements do not exceed the standard value V1 and the count memory is not N to the corresponding areas in the data memory 14, see page 9, [0016]). In page 11, [0021]-[0023], it also sets forth motivation to extrapolate the output of picture element having saturated during accumulation can be obtained late, and the dynamic rang of image sensor itself can be drastically expanded.

Allowable Subject Matter

9. Claims 7-8 and 18-20 objected to as being dependent upon a rejected base claim 1, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
10. Claims 24-30 are allowed.
11. The prior art does not teach or fairly suggest an image sensor comprising a sensor array that outputs signals representing one or more images according to claim 24 comprising a

multiplexer having a select input, first and second data inputs, and a data output; applying contents of the threshold memory to the select input; applied contents of the first and second buffers each to a different one of the first and the second data inputs of the multiplexer; controlling with the threshold memory the multiplexer to select the new data from the second buffer if the predetermined threshold is exceeded; controlling with the threshold memory the multiplexer to select the data read out of a row of the data memory data from the second buffer if the predetermined threshold is not exceeded; and providing a data output of the multiplexer which comprises an updated row of memory in which only values in those locations in the row that are to be updated have been changed.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

    a. Silverbrook et al. U.S. 6,614,560 discloses in Figure 15, a CMOS sensor is fabricated in an integrated circuit and 12Mbit DRAM data memory.

    b. O'Connor et al. U.S. 6,330,030 discloses in Figures 1-3, an image sensor comprising: a sensor array (the sensor array 32 includes a plurality of pixel capture circuit 50) that outputs signals representing one or more images (outputs from each of photosensor 52 in each times by counter 62) of a scene.

    c. Tsai U.S. Patent 5,309,243 discloses a method for extending the dynamic rang of an electronic imaging system.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Lin Ye
September 7, 2004